CLAIMS

1. An integrated circuit active memory device comprising:

a memory device having a data bus containing a plurality of data bus bits;

an array of processing elements each of which is coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements;

an array control unit being operable to generate a sequence of array control unit instructions responsive to each of a plurality of array control unit commands applied to a command input of the array control unit;

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit;

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands applied to a task command input of the command engine; and

a vector processing and re-ordering system coupled to the array control unit and the memory device, the vector processing and re-ordering system being operable to receive data from the memory device that may be stored in the memory device in other than a contiguous manner, re-order received data into a vector of contiguous data, process the data in accordance with an instruction received from the

array control unit to provide results data, and pass the results data to the memory device.

2. The active memory device of claim 1 wherein the memory device comprises a dynamic random access memory device.

3. The active memory device of claim 1, wherein the vector processor comprises:

a processing subsystem having a program memory storing a plurality of instructions, a command input coupled to the array control unit to receive the instruction from the array control unit, a data input operable to receive data to be processed, a data output operable to output processed data, and a processing unit coupled to the program memory, the data input and the data output, the processing unit being operable to process the data received at the data input in accordance with instructions stored in the program memory selected by an instruction received from the array control unit and to output the processed data to the data output; and

a data re-ordering subsystem operable to receive the data from the memory device, re-order received data into a vector of contiguous data, and couple the re-ordered data to the processing system, the data re-ordering system further being operable to and pass the results data to the memory device.

4. The active memory device of claim 3 wherein the data re-ordering system comprises an exchange unit that receives instructions from the array control unit to re-order the data from the memory device in accordance with the instructions.

5. The active memory device of claim 4, further comprising a multiplexer coupled to receive data from the exchange unit, the multiplexer receiving a

select signal that selects corresponding portions of the data received from the exchange unit.

6. The active memory device of claim 3 wherein the data re-ordering subsystem is further operable to re-order the results data prior to passing the results data to the memory device.

7. The active memory device of claim 1 wherein the vector processing and re-ordering system comprises:

a vector register coupled to receive data from the memory device and to transmit data to the memory device;

a vector memory coupled to the vector register to store data transferred from the vector register and to pass data stored in the vector memory to the vector register; and

a vector processor coupled to the vector memory to receive data from the vector memory for processing and to pass results data to the vector memory.

8. The active memory device of claim 7, further comprising an addressing engine coupled to the vector memory, the addressing engine being operable to control the locations in which data are stored in the vector memory.

9. The active memory device of claim 8 wherein the addressing engine is operable to selectively control an address sequence applied to the vector memory as data are coupled to or from the vector memory to re-order the data coupled to or from the vector memory.

10. The active memory device of claim 7 wherein the vector memory comprises a dual-ported memory, one of the ports of the vector memory being coupled

to the vector register and the other of the ports of the vector memory being coupled to the vector processor.

11. The active memory device of claim 7 wherein the vector memory comprises a random access memory.

12. The active memory device of claim 7 wherein the vector processor comprises:

an arithmetic and logic unit; and

a register coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit.

13. A vector processing and re-ordering system, comprising:

a vector register receiving data that may be in other than a contiguous order;

a vector memory coupled to the vector register to store data transferred from the vector register and to pass data stored in the vector memory to the vector register; and

a vector processor coupled to the vector memory to receive data from the vector memory, the vector processor being operable to re-order the data received from the vector memory into a vector of contiguous data, process the data to provide results data, and pass the results data to the vector memory.

14. The vector processing and re-ordering system of claim 13, further comprising an addressing engine coupled to the vector memory, the addressing engine being operable to control the locations in which data are stored in the vector memory.

15. The vector processing and re-ordering system of claim 14 wherein the addressing engine is operable to selectively control an address sequence applied to the vector memory as data are coupled to or from the vector memory to re-order the data coupled to or from the vector memory.

16. The vector processing and re-ordering system of claim 13 wherein the vector memory comprises a dual-ported memory, one of the ports of the vector memory being coupled to the vector register and the other of the ports of the vector memory being coupled to the vector processor.

17. The vector processing and re-ordering system of claim 13 wherein the vector memory comprises a random access memory.

18. The vector processing and re-ordering system of claim 13 wherein the vector processor comprises:

an arithmetic and logic unit; and

a register coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit.

19. A computer system, comprising:

a host processor having a processor bus;

at least one input device coupled to the host processor through the processor bus;

at least one output device coupled to the host processor through the processor bus;

at least one data storage device coupled to the host processor through the processor bus; and

an active memory device, comprising:

a memory device having a data bus containing a plurality of data bus bits;

an array of processing elements each of which is coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements;

an array control unit being operable to generate a sequence of array control unit instructions responsive to each of a plurality of array control unit commands applied to a command input of the array control unit;

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit;

a command engine coupled to the host processor, the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands from the host processor; and

a vector processing and re-ordering system coupled to the array control unit and the memory device, the vector processing and re-ordering system being operable to receive data from the memory device that may be stored in the memory device in other than a contiguous manner, re-order received data into a vector of contiguous data, process the data in accordance with an instruction received from the array control unit to provide results data, and pass the results data to the memory device.

20. The computer system of claim 19 wherein the memory device comprises a dynamic random access memory device.

21. The computer system of claim 19, wherein the vector processor comprises:

a processing subsystem having a program memory storing a plurality of instructions, a command input coupled to the array control unit to receive the instruction from the array control unit, a data input operable to receive data to be processed, a data output operable to output processed data, and a processing unit coupled to the program memory, the data input and the data output, the processing unit being operable to process the data received at the data input in accordance with instructions stored in the program memory selected by an instruction received from the array control unit and to output the processed data to the data output; and

a data re-ordering subsystem operable to receive the data from the memory device, re-order received data into a vector of contiguous data, and couple the re-ordered data to the processing system, the data re-ordering system further being operable to and pass the results data to the memory device.

22. The computer system of claim 21 wherein the data re-ordering system comprises an exchange unit that receives instructions from the array control unit to re-order the data from the memory device in accordance with the instructions.

23. The computer system of claim 22; further comprising a multiplexer coupled to receive data from the exchange unit, the multiplexer receiving a select signal that selects corresponding portions of the data received from the exchange unit.

24. The computer system of claim 21 wherein the data re-ordering subsystem is further operable to re-order the results data prior to passing the results data to the memory device.

25. The computer system of claim 19 wherein the vector processing and re-ordering system comprises:

a vector register coupled to receive data from the memory device and to transmit data to the memory device;

a vector memory coupled to the vector register to store data transferred from the vector register and to pass data stored in the vector memory to the vector register; and

a vector processor coupled to the vector memory to receive data from the vector memory for processing and to pass results data to the vector memory.

26. The computer system of claim 25, further comprising an addressing engine coupled to the vector memory, the addressing engine being operable to control the locations in which data are stored in the vector memory.

27. The computer system of claim 26 wherein the addressing engine is operable to selectively control an address sequence applied to the vector memory as data are coupled to or from the vector memory to re-order the data coupled to or from the vector memory.

28. The computer system of claim 25 wherein the vector memory comprises a dual-ported memory, one of the ports of the vector memory being coupled to the vector register and the other of the ports of the vector memory being coupled to the vector processor.

29. The computer system of claim 25 wherein the vector memory comprises a random access memory.

30. The computer system of claim 25 wherein the vector processor comprises:

an arithmetic and logic unit; and

a register coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit.

31. A method of storing and processing data in an integrated circuit, the method comprising:

storing data in an array of memory cells in the integrated circuit;

in response to a memory command, reading data from the memory cells in the integrated circuit;

re-ordering the data read from the memory cells in the integrated circuit, the re-ordering occurring in the integrated circuit; and

processing the re-ordered data in the integrated circuit.

32. The method of claim 31, further comprising writing the processed data to the memory cells in the integrated circuit.

33. The method of claim 31 wherein the memory cells comprises dynamic random access memory cells.

34. The method of claim 31 wherein the act of processing the re-ordered data in the integrated circuit comprises parallel processing the re-ordered data.

35. The method of claim 34 wherein the act of parallel processing the re-ordered data comprises single instruction, multiple data processing of the re-ordered data.

36. The method of claim 35 wherein the act of processing the re-ordered data in the integrated circuit comprises separately processing data read from respective groups of columns of memory cells.

37. The method of claim 31 wherein the act of re-ordering the data read from the memory cells in the integrated circuit comprises selecting predetermined portions of the data read from the memory cells.

38. The method of claim 31 wherein the act of storing data in an array of memory cells in the integrated circuit comprises coupling the data to the array of memory cells from an external data port.

39. In an integrated circuit active memory device having an array of memory cells and an array of processing elements each of which is coupled to a respective group of the memory cells, a method of processing data in the active memory device, comprising re-ordering data read from the memory cells in a predetermined manner before processing the data in the integrated circuit active memory device to obtain results data.

40. The method of claim 39, further comprising:

re-ordering the results data; and

storing the re-ordered results data in the memory cells.